REMARKS

Claims 1-36 are currently pending, of which claims 1, 19, and 26 are in independent form. Claims 1, 3, 19, and 26 have been amended hereby. No new matter is introduced.

Favorable reconsideration of the present patent application as currently constituted is respectfully requested.

Regarding Amendments to the Specification

Paragraph [0001] of the original specification has been amended to include updated information regarding the cross-referenced related applications.

Regarding the Claim Objections and Allowable Subject Matter

Claim 26 has been amended to rectify the typographical error pointed out in outstanding Office Action.

Applicant gratefully appreciates the indication of allowable subject matter. In particular, it is indicated that claims 19-36 are allowed. Further, claims 3-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant has amended the base claim 1 to distinguish over the applied art of record, as will be discussed in detail below. Accordingly, Applicant respectfully submits that base claim 1 as well as claims 2-18, which depend from claim 1 and add further limitations therein, are also in condition for allowance.

Regarding the Claim Rejections - 35 U.S.C. §102(b)

In the pending Office Action, claim 1 is rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,548,620 to Rogers (hereinafter the *Rogers* reference). The following comments were provided with respect to this §102 rejection:

> Rogers discloses a method of transferring data from circuitry disposed in a first frequency clock domain to circuitry disposed in a second frequency clock domain, said first frequency clock domain operating with a first clock signal [SLOW] and said second frequency clock domain operating with a second clock signal [FAST], comprising the steps:
>
> latching said data in a first latch [element 214 in Figure 2] to generate a first latched data output, said first latch operating in response to a first modified clock signal [SLOW_R] that is synthesized at least in part from said first clock signal [column 4, lines 56-65];
>
> providing said first latched data output to a second latch [element 222 in Figure 2] disposed in said second frequency clock domain, wherein said second latch is gated by a second modified clock signal [FAST_R] synthesized at least in part from said second clock signal, said second latch operating to generate a second

latched data output [column 4, lines 35-43 and Figure 3]; and

providing said second latched data output to a register [element 224 in Figure 2] clocked by said second clock signal [FAST] for generating a synchronized data output [DATA OUT in Figure 2] operable to be supplied to said circuitry disposed in said second frequency clock domain [column 5, lines 8-18].

Rogers discloses a method for transferring data from a first, slower, clock frequency domain to a second, higher, clock frequency domain. Rogers also states that the same technique can be applied to transfer data from a first, higher, clock frequency domain to a second, lower, clock frequency domain [column 5, lines 34-43]. Therefore, Rogers discloses using the method described above, to transfer data from a higher frequency clock domain to a lower frequency clock domain.

Applicant respectfully submits that the pending §102 rejection has been overcome or otherwise rendered moot by the present amendment. As currently constituted, the base claim 1 recites a modified clock signal synthesized based on a plurality of intermediary clock signals that are generated at least in part from a faster, first clock signal. In contrast, the *Rogers* reference discloses a FAST_R signal that is merely a regenerated single clock signal referred to as FAST. See Figures 3, 4 and 5; see also col 4, lines 35-43; col. 5, lines 42-52; and col. 7, lines 26-36. It is respectfully contended that the FAST_R signal does not anticipate or even remotely suggest Applicant's modified clock

signal that is synthesized based a plurality of intermediary clock signals as currently claimed.

Regarding the Claim Rejections - 35 U.S.C. §103(a)

In the pending Office Action, claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over the *Rogers* reference in view of U.S. Patent No. 6,345,328 to Rozario et al. (hereinafter the *Rozario* reference). The following comments were provided with respect to this §103 rejection:

> Rogers discloses a method of transferring data from a first, higher, clock frequency domain to a second, lower clock frequency domain, but does not specifically state that the first and second clock signals are provided at a ratio of [N:M], where N equals the number of cycles of said first clock signal and M equals the number of cycles of said second clock signal and further equals (N-1). However, Rozario discloses that it is well known in the art to transfer data from a conventional core clock frequency domain [CCLK at 133 MHz] to a conventional peripheral clock frequency domain [PCLK at 66MHz, column 5, lines 35-51 and column 6, lines 16-18]. The ratio between the conventional CCLK and PCLK domains is [2:1].

Applicant respectfully submits that the pending §103 rejection has been overcome or otherwise rendered moot by the present amendment. As set forth in the foregoing discussion, the *Rogers* reference is critically deficient when applied as a reference against the base claim 1. Application of the *Rozario* reference,

however, is of no avail in curing the deficiency of the primary reference, i.e., the *Rogers* reference, when combined as a basis for obviousness. It is well known that to establish obviousness, three basic criteria must be met. First, there must be some suggestion or motivation to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the combined references must teach or suggest all the claim limitations. See MPEP §2143. Applicant respectfully contends that there is no suggestion or motivation in either of the applied references to combine the teachings therein so as to achieve the claimed invention directed to a method of transferring data from circuitry disposed in a higher frequency clock domain to circuitry disposed in a lower frequency clock domain, which involves a modified clock signal synthesized based on a plurality of intermediary clock signals that are generated at least in part from a faster, first clock signal. The *Rozario* reference's objective to provide gear box circuitry for transferring data between synchronous sequential logic circuits, each having their own clock domain, whereby metastability is avoided and timing delays associated with the transfer are reduced. Col. 2, line 66 to col. 3, line 7. As described, gear box module 300 includes latch 330, MUX 340, and an AND gate 350. See Figure 3; see also

col. 7, line 5 et seq. Flip-flops 360 and 370, as well as combinational delays 365 and 375 illustrate digital circuitry present in two clock domains, between which the gear box module 300 is disposed. Applicant respectfully submits there is not even a scintilla of motivation or suggestion in the combined teachings of the *Rogers* and *Rozario* references with regard to providing a modified clock signal derived from a plurality of intermediary clock signals as claimed by Applicant. Accordingly, it is believed that claim 2, which depends from the base claim 1 and introduces additional limitations therein, is allowable over the applied art of record.

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SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the present invention, as now defined by the independent claims, and in further view of the above amendments and remarks, reconsideration of the Action and allowance of the present invention are respectfully requested and are believed to be appropriate.

Respectfully submitted,

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